UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 2:22-cv-203-JRG JURY TRIAL DEMANDED

NETLIST INC.'S OBJECTIONS TO CLAIM CONSTRUCTION MEMORANDUM ORDER

For purposes of preserving issues for appeal, Plaintiff Netlist, Inc. ("Netlist") respectfully objects to the Claim Construction Order dated October 21, 2023 (Dkt. 249).

I. "drive" ('339, all claims)

For at least the reasons set out in Netlist's opening and reply claim construction briefs and at oral argument, the Court erred in construing the "drive" to mean "to enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled." Dkt. 249 at 43; Dkt. 97 at 9-12; Dkt. 110 at 5-6. The Court previously construed "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," which was the correct construction of the "drive" terms. Dkt. 97-08 (December 14, 2022 Claim Construction Order in *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, Case No. 2:21-cv-463), at 34.

The October 21, 2023 claim construction order erred in further construing the "drive" terms in at least two ways. First, the Court erred by excluding read paths from the "other possible paths" that could be disabled during a write operation. Dkt. 249 at 25-26, 43. The '339 patent claims a configuration in which the data paths in the data buffer are closed when the memory module is not communicating data with the memory controller, which is reflected in the prosecution history. *See, e.g.*, '339, 19:56-61 ("wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, ***wherein the byte-wise data path is enabled for a first time period*** in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period"); Dkt. 97-8 at 9-10 ("controlling the data paths between the memory devices and the bus interface so that the data paths are open for a time period to allow data to be driven between the memory devices and the memory controller" without limitation as to specific read or write path) (quoting Netlist's Mar. 25, 2020 Resp. to Office Action). Second, the Court erred by construing

the "drive" terms as requiring enabling data paths corresponding to "the respective byte-wise section of the N-bit wide write data" and disabling data paths corresponding to "the same respective byte-wise section of the N-bit wide write data." Dkt. 249 at 26. The claims distinguish between "byte wise" and "byte wide." The specification teaches an embodiment where the "byte-wise" data path through the buffer can be a half-byte (i.e., nibble or four bit) data paths. *See* '339 patent, 13:54-63 (in preferred embodiments Figs. 3B and 4B, a byte-wise section of the N-bit wide data is transferred over two 4-bit paths). The specification explains that the "byte-wise buffer" depicted in Fig. 4B "selectively transmits data bits 0-3 to a first memory device … and data bits 4-7 to a second memory device." *Id.*, 14:1-17; *see also id.*, 14:15-34 (in some embodiments, "not all the [data] bits are grouped together and not all the bits produce the same behavior (e.g., logic- and/or time-wise)").

Furthermore, the specification does not limit the possible data path for a byte-wise section of N-bit wide data to only those passing through the same data buffer on the same memory module. For example, the specification teaches an embodiment where four memory modules are connected to the same memory controller. '339, 17:14-17:44.[1] The specification teaches that when one particular rank—which is associated with a particular memory module—is selected, the data buffers on non-selected memory modules are all disabled. *Id.*, '339, 17:17-24. That is, all those possible data paths are disabled. Thus, to the extent that the construction excludes these possible data paths, that is another reason for objecting to the construction.

[1] As a preliminary matter, a data buffer would provide load reduction even when there is a single data path. For example, without the data buffer, two single ranks on the same path would present two loads. *See* '339, 5:44-64. A single load is obtained with the write buffer 503 and the read buffer 509 in the data buffer. *E.g.*, '339, 16:45-64. That is, the '339 patent's inventions are not limited to configurations with "forks" in the road; and where there are more than two possible paths, the load experienced by the memory controller or experienced the memory devices would be one load per memory module regardless of the number of paths enabled or disabled. *E.g.*, '339, 17:14-44 (memory controller experiences four loads even when the data buffers and data paths on three of the four memory modules are disabled).

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a).

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